# M.Tech (Electronics Engineering) Scheme of Examination

## Semester I

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Sub Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Total Contact Hours</th>
<th>Credits</th>
<th>MSE - I</th>
<th>MSE - II</th>
<th>TA</th>
<th>ESE</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EE901</td>
<td>Advanced Digital Signal Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>2</td>
<td>EE902</td>
<td>Digital IC Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>3</td>
<td>EE903</td>
<td>RISC &amp; DSP Processor Architecture</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>4</td>
<td>EE904</td>
<td>Advanced Digital System Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>5</td>
<td>EE905</td>
<td>Advanced Communication Systems</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>6</td>
<td>EE906</td>
<td>Advanced Digital Signal Processing Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>7</td>
<td>EE907</td>
<td>Digital IC Design Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>8</td>
<td>EE908</td>
<td>Advanced Digital System Design Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
</tbody>
</table>

**Total Credits:** 150

## Semester II

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Sub Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Total Contact Hours</th>
<th>Credits</th>
<th>MSE - I</th>
<th>MSE - II</th>
<th>TA</th>
<th>ESE</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EE911</td>
<td>RF Circuit Design</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>2</td>
<td>EE912</td>
<td>Soft Computing Techniques</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>3</td>
<td>EE913</td>
<td>Digital Image Processing</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>4</td>
<td>Elective 1</td>
<td></td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>5</td>
<td>Elective 2</td>
<td></td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>6</td>
<td>EE914</td>
<td>Digital Image Processing Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>7</td>
<td>EE915</td>
<td>RF Circuit Design Laboratory</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
</tbody>
</table>

**Total Credits:** 124

## Semester III

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Sub Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Total Contact Hours</th>
<th>Credits</th>
<th>MSE - I</th>
<th>MSE - II</th>
<th>TA</th>
<th>ESE</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Elective 3</td>
<td></td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>2</td>
<td>Elective 4</td>
<td></td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td>6</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
<tr>
<td>3</td>
<td>EE931</td>
<td>Project Phase - I</td>
<td>0</td>
<td>0</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>3 Hrs</td>
</tr>
</tbody>
</table>

**Total Credits:** 70

## Semester IV

<table>
<thead>
<tr>
<th>Sl.No.</th>
<th>Sub Code</th>
<th>Subject</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>Total Contact Hours</th>
<th>Credits</th>
<th>MSE - I</th>
<th>MSE - II</th>
<th>TA</th>
<th>ESE</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>EE941</td>
<td>Project Phase - II</td>
<td>0</td>
<td>0</td>
<td>20</td>
<td>20</td>
<td>20</td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>100</td>
</tr>
</tbody>
</table>

**Total Credits:** 116
OBJECTIVES
To acquaint students with advanced methods of digital signal processing and their application in practice. Design and testing of systems for advanced signal processing, aiming at optimum and adaptive noise reduction, identification and modelling of systems, reconstruction and restoration, analysis and classification of signals and images.

UNIT I
Z- Transform: Linear Time Invariant system in Z domain, Discrete Fourier transform, Fast Fourier transform.

UNIT II

UNIT III
Structures for the realization of discrete Time system: Ladder, lattice structure for FIR system. State space system analysis and structures, finite word length effect.

UNIT IV
Linear prediction and optimum linear filters: forward and backward linear prediction, AR Lattice and ARMA lattice – ladder filters, Wiener filters for filtering on prediction.

UNIT V
Multirate DSP: Decimation by a factor D – Interpolation by a factor I – Filter Design and implementation for sampling rate conversion, Polyphase filter structure.

UNIT VI
Parametric signal modeling: Auto regressive signal modeling based on linear prediction, pole zero modeling. Time varying auto regressive models. Parametric signal modeling in the presence of noise. applications, spectral analysis. Power spectral analysis using DFT.

References:
**OBJECTIVES**

The aim of this course is to give knowledge and skills in the area of CAD design of digital circuits, units and systems on currently usable VLSI chips.

**Unit – I: CMOS processing technology:**
MOS transistors, CMOS logic, NAND gate, combinational logic, NOR gate, Compound gates, Pass transistor and transmission gates, tristates, multiplexers, latches and flip flops, inverter cross section, fabrication process, Layout design rules, CMOS processing technology, CMOS Process enhancements, stick diagram, VLSI design flow, Euler path in a CMOS gate.

**Unit - II :MOS transistor theory:**
MOS transistor theory, Working of nMOS enhancement transistor & PMOS enhancement transistor, Ideal Current voltage characteristics, threshold voltage, nonideal current voltage effects, velocity saturation, mobility degradation, channel length modulation, Body effect, subthreshold conduction, Junction leakage, Tunneling, Temperature dependence, Geometry dependence, Small signal AC characteristics, CMOS inverter DC transfer characteristics, Beta ratio effects, noise margin, Ratioed inverter transfer function, switch level RC delay models.

**Unit - III :Circuit characterization and performance estimation:**
Delay estimation, RC delay models, linear delay model, logical effort, parasitic delay, Delay in a logic gate, delay in a multistage logic networks, power dissipation, interconnect, design margin, Reliability, Scaling.

**Unit – IV:Combinational circuit design:**
Circuit families ,static CMOS, Ratioed circuits, Cascode voltage switch logic, dynamic circuits, pass transistor circuits, differential circuits, sense amplifier circuits, BiCMOS circuits.

**Unit – V: Sequential Circuit design:**
Sequencing static circuits, Sequencing methods, Max-delay constraints, Min-delay constraints, Time borrowing, clock skew, circuit design of latches and Flip flops, static sequencing element methodology, Two phase timing types, characterizing sequencing element delays, sequencing dynamic circuits, Synchronizers.

**Unit – VI: Array subsystems:**
Static Random access memory, Dynamic random access memory, serial access memories, Content addressable memory Programmable logic arrays.

**References**

OBJECTIVES
The aim of this course is to give knowledge and skills in the area of embedded system particularly RISC architecture & develop a system around processor core particularly ARM core.
Also this subject will provide knowledge about DSP Processors and associated hardware experimentation.

Unit - I
Introduction to Embedded Systems, Processor Technology, IC Technology, Design Technology, Design Productivity Gap, RISC architecture, CISC architecture, Von Neuman & Harward architecture, Simple Processor Design, RT level organisation. Instruction set design, pipelining

Unit - II
Architectural Features of ARM: Processor modes, Register organization, ARM exceptions, ARM and THUMB instruction sets, Programming, ARM development tools.

Unit - III
Pipeline ARM organisation, ARM instruction execution, ARM implementation, Design of architecture blocks at RTL level, Timing diagrams for data path, Co-processor interface, Hardware and software breakpoints, Exceptions and its handling, Memory faults

Unit - IV
ARM architectural support for high level language programming, floating point data types, functions and procedures, Thumb instruction set. The ARM memory interface, the advanced buses: AMBA, ASB, APB, ARM Debugger, embedded ARM application: GSM chip organisation & handset architecture.

Unit - V
DSP Architecture: MAC, Modified bus structures and Memory access schemes, Multiple access Memory, Multi-ported memory, VLIW architecture, Pipelining, Special addressing modes, 32 bit floating point DSP Processor: architecture, block diagram, functional units, on chip memory, on chip peripherals.

Unit - VI
Assembly language programming: Instruction set, addressing modes, programming, Hardware tools: DSP and other DSP boards Software tools: Assembly language tools, DSP simulator, C compiler and C source debugger, Simmons, works with a DSK.

References:
4. Technical reference manuals from TI
OBJECTIVES
To expose students to the advanced design techniques and methodology and industrial standard EDA tools in Digital Circuits and Systems design.

Unit - I
Digital Design Fundamentals, Combinational & Sequential design issues, Introduction to finite state machines, Moore & Mealy Machine, Introduction to programmable devices, PLA, PAL, PROM, Structure of CPLDs, Introduction to FPGA, Architecture, CLB, IOB, Programmable Interconnect Points, Different type of programmable switches used in PLDs

Unit - II
HDL Based Design flow, Requirements of HDL, Design Methodologies, Different Modelling styles, Introduction to Verilog, Elements of Verilog, Verilog Module definition, Elements of Module

Unit – III
Basic Concepts in Verilog, Reserved Keywords, Syntax & Semantics, Comments, Identifiers, Number Representation, System Representation, Verilog Ports, Verilog Data Types, Wire & Variables, Physical & Abstract, Constants, Parameter, Verilog Data Operators, Design entry in Verilog & Testbench, Compilation and synthesis, Timing analysis

Unit – IV
Data Flow Modelling, Delay, Continuous Assignment, Delayed Continuous assignment, Structural Modelling Feature, Module Instantiation, Gate level Primitives, Gate Delays, Switch Level Primitives, User Defined Primitives

Unit - V
Behavioral Modelling, Initial, Always, Procedural Assignment, Blocking and Non- Blocking assignments, Sequential & Parallel Blocks, Race around Condition, Timing Control, Procedural Statements, Conditional Statements if case loop repeat forever etc, Zero Delay Control, Event Based Timing Control, Compiler Directives, Assign Deassign, Force Release, Latch Models, FF Models, State Machine Coding ,Moore and Mealy Machines

Unit - VI
Combinational & sequential system Design examples like Shift Registers, Counters, LFSR, Stacks and Queues, Multi bit Adders & Multiplier, Huffman Coding, Processor and Memory Model , CPU, System Tasks and Functions, Design Verification

References:
OBJECTIVES
To acquaint students to the advanced communication systems and methodology and various issues related with Communication.

Unit - I
Review of Random variable: Moment generating function, Chernoff bound, Markov's inequality, Chebyshev's inequality, Central limit Theorem, Chi square, Rayleigh and Rician distributions, Correlation, Covariance matrix.

Unit - II
Characterization of Communication Signals and Systems - Signal space representation - Vector space concept, signal space concept, orthogonal expansions of signals, representation of digitally modulated signals - memory less modulation methods, linear modulation with memory, nonlinear modulation methods with memory.

Unit - III
Optimum waveform receiver in additive white Gaussian noise (AWGN) channels - Cross correlation receiver, Matched filter receiver and error probabilities. Optimum Receiver for Signals with random phase in AWGN Channels. Optimum receiver for M-ary orthogonal signals. Optimum waveform receiver for coloured Gaussian noise channels

Unit – IV.
Channel Capacity and Convolutional Coding: Channel models, Channel Capacity, Transfer convolutional Codes, Optimum decoding of convolutional codes - Viterbi algorithm, Fano algorithm, Punctured convolutional codes.

Unit - V

Unit - VI
Communication over band limited Channels - Optimum pulse shaping - Nyquist criterion for zero ISI, partial response signalling - Equalization Techniques - Zero forcing linear Equalization - Decision feedback equalization-

References:
3. "Digital Communication", Simon Haykins
OBJECTIVES
Practical's based on syllabus of Advanced Digital Signal Processing (EE901)
OBJECTIVES

Practical's based on syllabus of Digital IC Design (EE902)
### Evaluation Scheme

<table>
<thead>
<tr>
<th>Continuous Evaluation</th>
<th>ESE</th>
<th>Total</th>
<th>ESE Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>40</td>
<td>60</td>
<td>100</td>
<td></td>
</tr>
</tbody>
</table>

**OBJECTIVES**

Practicals based on syllabus of *Advanced Digital System Design.*
OBJECTIVES
To study RF component such as resonator, filter, transmission lines, etc, 
To learn design of RF amplifiers using transistors

Unit – I

Unit – II

Unit – III
An Overview of RF Filter Design, Basic Resonator and Filter Configurations, Special Filter Realizations, Filter Implementation, Coupled Filter.

Unit – IV

Unit – V

Unit – VI
RF Transistor Amplifier Designs: Characteristics of Amplifiers, Amplifier Power Relations, Stability Considerations, Constant Gain, Noise Figure Circles, Constant VSWR Circles, Broadband, High-Power, and Multistage Amplifiers, Oscillators and Mixers Basic Oscillator Model, High-Frequency Oscillator Configuration, Basic Characteristics of Mixers.

References:
EE 912 | Soft Computing Techniques | L = 3 | T = 0 | P = 0 | Credits = 6

<table>
<thead>
<tr>
<th>Evaluation Scheme</th>
<th>MSE-I</th>
<th>MSE-II</th>
<th>TA</th>
<th>ESE</th>
<th>Total</th>
<th>ESE Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15</td>
<td>15</td>
<td>10</td>
<td>60</td>
<td>100</td>
<td>3 Hrs</td>
</tr>
</tbody>
</table>

OBJECTIVES
To introduce the ideas of fuzzy sets, fuzzy logic and use of heuristics based on human experience & neural networks that can learn from available examples and generalize to form appropriate rules for inferencing systems. To provide the mathematical background for carrying out the optimization associated with neural network learning To familiarize with genetic algorithms and other random search procedures useful while seeking global optimum in self-learning situations

Unit - I
Fuzzy sets- Basic concepts, representation of fuzzy sets, fuzzy complements, t- Norms, t- Co-norms, Aggregation operations [6Hrs]

Unit - II
Fuzzy arithmetic, Arithmetic operations on intervals and fuzzy numbers, fuzzy equations, Fuzzy relations, Fuzzy expert systems, Fuzzy controllers [7Hrs]

Unit - III
Introduction to neural networks, Neural Network architectures and learning processes, Single and Multi-layer perceptrons, Feedback networks-Discrete and continuous Hopfield nets, [7Hrs]

Unit - IV
Feed-forward nets- Back propagation network, Radial Basis Function networks, Self organizing maps-Kohonen SOM, Learning vector quantization, MAX net, Maxican Hat, Hamming net [7Hrs]

Unit – V
Basic concepts of Genetic Algorithms, working principle, methods of encoding, fitness function and reproduction. [6Hrs]

Unit – VI

References:
OBJECTIVES
Provide deeper knowledge of theoretically demanding methods of image data processing and of their applications.

Unit - I

Unit - II
Spatial domain methods, Frequency domain methods, Histogram Modification technique, Neighbourhood averaging, Median filtering, Low pass filtering, Averaging of Multiple Images, Image sharpening by differentiation, High pass Filtering,

Unit - III
Degradation model for Continuous functions, Discrete Formulation, Diagonalization of Circulant and Block – Circulant Matrices, Effects of Diagonalization, Constrained and unconstrained Restorations Inverse filtering, Wiener Filter, Constrained least Square Restoration.

Unit - IV
Fundamentals, Image compression models, error free compression, lossy compression, image compression standards Objective an subjective Fidelity Criteria, the encoding process, the Mapping, the Quantizer and the Coder, Contour Encoding, Run length Encoding, Image Encoding relative to a Fidelity Criterion, Differential Pulse Code Modulation, Transform Encoding.

Unit - V
The detection of Discontinuities, Point Line and Edge Detections, Gradient Operators, Combined Detection, Thresholding. Representation Schemes, Chain Codes, Polygon Approximation, Boundary Descriptors, Simple Descriptors, Shape Numbers, Fourier Descriptors Dilation and erosion, opening and closing hit-or-miss transformation, morphological algorithms, extension to gray scale images.

Unit - VI
Wavelets and multiresolution processing, Sub-band coding, Multiresolution expansion, One dimensional wavelet transform, Wavelet series expansion, Discrete wavelet transform, Continuous wavelet transform, fast wavelet transform, 2-D wavelet transform, Wavelet packets.

References:
**OBJECTIVES**
To expose students to the advanced Power Electronics, Controlled Rectifiers, Chopper, Advanced Converters.

**Unit – I**
Power Semiconductor Devices, Overview of power semiconductor devices – SCR, BJT, IGBT, MOSFET, & IGCT their characteristics, ratings & protection

**Unit – II**
Controlled Rectifiers, Single Phase & Three Phase full Converters with R & R-L load, Single phase & three phase dual converters, Power factor improvement techniques.

**Unit - III**
D.C to D.C. Converters, Chopper Classification, Thyristor Chopper Circuits, Types of Converters and their controls

**Unit - IV**
Inverters, Principle of Operation, Performance parameters, single phase bridge invertors and their voltage Control, Harmonic Reduction, types of PWM techniques, different methods to control output voltage.

**Unit – V**
Advanced Converters, Multi level converter, Resonant converters, Basic of cycloconverter, Matrix converter, Front end rectifier

**Unit – VI**
Electric Utility Applications, Power conditioners and uninterrupted power supplies (UPS), protection of supply

**References :**

7. Related IEEE/IEE Publication
OBJECTIVES
To acquaint the students with Multirate systems, Multirate Filter Banks and wavelet transform and application in signal processing

Unit I
Basic multi-rate operations, interconnection of building blocks, poly-phase representation, multistage implementation, applications of multi-rate systems, special filters and filter banks.

Unit II
Maximally decimated filter banks: Errors created in the QMF bank, alias free QMF system, power symmetric QMF banks, M-channel filter banks, poly-phase representation, perfect reconstruction systems, alias-free filter banks

Unit III
Para-unitary Perfect Reconstruction Filter Banks: Lossless transfer matrices, filter bank properties induced by paraunitariness, two channel Paraunitary lattices, M-channel FIR Para-unitary QMF banks, transform coding.

Unit IV
Linear Phase Perfect Reconstruction QMF Banks: Necessary conditions, lattice structures for linear phase FIR PR QMF banks, formal synthesis of linear phase FIR PR QMF lattice., tree structured filter banks, trans-multiplexers.

Unit V
Pseudo-QMF bank. Short-time Fourier transform: trades of between traditional Fourier transform and STFT, STFT as a bank of filter, window selection, STFT versus Wavelet transform, STFT to wavelet conversion, basic wavelet.

Unit VI
Discrete-time Ortho-normal wavelets, Continuous-time Ortho-normal wavelets.

REFERENCE BOOKS:
<table>
<thead>
<tr>
<th>Evaluation Scheme</th>
<th>MSE-I</th>
<th>MSE-II</th>
<th>TA</th>
<th>ESE</th>
<th>Total</th>
<th>ESE Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>15</td>
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**OBJECTIVES**

To acquaint students with principles of design, analysis, modelling and optimization of low power VLSI, as well as to promote an interest in VLSI design

**Unit - I**

Need for low power VLSI chips, Sources of power dissipation: Short circuit dissipation, dynamic dissipation, designing Techniques for low power. Physics of power dissipation in MOSFET devices, The MIS Structure. Basic principle of low power design, low power figure of merits, brief overview of low power VLSI design limits, Gate level logic simulation, architecture-level analysis.

(6 hours)

**Unit - II**

Probabilistic power analysis: random logic signals, probability and frequency, probabilistic power analysis techniques, signal entropy, Low power circuits: transistor and gate sizing, equivalent pin ordering, network reconstruction and reorganization, special latches and flip-flops.

(7 hours)

**Unit - III**

Behavioral, Logic and circuit level approaches. Algorithm level transforms. Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre-computation, Logic: gate reorganization, signal gating, logic encoding, state machine encoding, Transistor sizing.

(6 hours)

**Unit - IV**

Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect. Low voltage design techniques using reverse Vgs. Steep sub threshold swing and multiple threshold voltages. Multiple threshold CMOS based on path critically, multiple supply voltages.

(6 hours)

**Unit - V**

Low energy computing, Energy dissipation in transistor channel. Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and IO Buffer, supply clock generation.

(6 hours)

**Unit - VI**

Introduction, sources of software power dissipation, power estimation and optimization. Co-design for low power.

(4 hours)

**References:**

OBJECTIVES

The course aims to give basic knowledge of different mobile / wireless communication systems

Unit - I

Unit - II
The Cellular Concept: Cell Area, Signal strength & cell parameters, capacity of a cell, Frequency reuse, cochannel interference, cell splitting & cell sectoring, Evolution of mobile radio communication, Cellular telephone system, channel assignment and handoff strategies, interference and system capacity, trunking and grade of service, improving capacity in cellular system.

Unit - III

Unit - IV
Wireless communications through fading multipath channels, effect of signal characteristics on the choice of channel model, signalling over frequency selective fading channel, coded waveforms

Unit - V
Equalization & Diversity: Fundamentals of equalization, space polarization, frequency and time diversity techniques, space diversity, polarization diversity, frequency and time diversity. RAKE Receiver

Unit - VI
Wireless Systems and Standards: GSM- global system for mobile: services and features, GSM system architecture, GSM radio subsystem, GSM channel types, GSM frame structure, signal processing in GSM, introduction to CDMA digital cellular standard (IS-95).

References:
OBJECTIVES
The students shall gain proficiency in subjects like the basic design of theory involved in VLSI for signal processing and communication systems, various software tools related to VLSI, Signal Processing and Communication Systems.

UNIT I:
Introduction to DSP systems, Data flow and Dependence graphs - critical path, Loop bound, iteration bound, longest path matrix algorithm, Pipelining and Parallel processing of FIR filters, parallel processing, Pipelining and parallel processing for low power.

(6 hours)

UNIT II:
Retiming – definitions and properties, solving systems of inequalities, Retiming techniques, Unfolding – an algorithm for unfolding, properties of unfolding, sample period reduction and parallel processing application

(7 hours)

UNIT III:
Folding: folding transformation, Register Minimization Techniques, Register minimization in folded architectures folding of multirate systems. Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix Multiplication and 2D systolic array Design, Systolic design for space representations containing Delays.

(7 hours)

UNIT IV:

(7 hours)

UNIT V:

(6 hours)

Unit VI:

(7 hours)

REFERENCES:


OBJECTIVES
To gain a knowledge from the area of applying diagnostic principles in the design of modern electronic systems.

Unit - I

Unit - II

Unit - III

Unit - IV
More Test Generation and D-algorithm D-algorithm, representation, cube algebra, generalized algorithm, Extensions to Dalgorithm PODEM, FAN, etc. Random test generation, Complexity issues Functional Test Generation Methods, Heuristic Methods, Exhaustive and Pseudo Exhaustive techniques

Unit - V

Unit - VI
Scan Design, Scan Designs: IEEE Standards, Board-Level Testing: Boundary Scan, Data Compression and BIST, LFSR polynomial generation Data compression techniques Aliasing Probability, BIST, Self Checking and PLD Testing

References:
OBJECTIVES
Practicals based on syllabus of Digital Image Processing

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EE 915 RF Circuit Design Laboratory  

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**OBJECTIVES**

Practicals based on syllabus of **RF Circuit Design**
EE 932 | Wireless Sensor | L = 3 | T = 0 | P = 0 | Credits = 6

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OBJECTIVES

The objective of the course is to give the student good understanding of programming embedded wireless systems where the requirements on low energy dissipation is hard and the real time requirements and the limited resources of memory and processing capability makes it necessary for optimised the implementation of the software functions.

Unit - I

Unit - II

Unit - III
Sensors Network Protocols, Data dissemination and gathering, Routing Challenges and design issues in wireless sensor network, Routing strategies in WSN.

Unit - IV
Protocols, Transport Control Protocols for Wireless Sensors Networks, Traditional transport control protocol, transport protocol design issues, examples of existing transport control protocol, performance of TCP.

Unit - V
Middleware for Sensor Networks, WSN middleware principles, Middleware architecture, existing middleware.

Unit - VI

References:
OBJECTIVES

To expose students to the advanced Electromagnetic & Electrodynamic techniques and methodology.

Unit – I
Mathematic Methods, Vectors (Ordinary Vectors, Pseudovectors, Complex Vectors), Fields, Vector Algebra, Vector Analysis, Analytical Mechanics, Classical Electrodynamics, Electrostatics, Magnetostatics, Electrodynamics, Electromagnetic Duality

Unit - II

Unit - III

Unit - IV
Electromagnetic Radiation and Radiation And Radiating Systems, Radiation From Extended Sources, Multipole Radiation, Radiation From A Localized Charge In Arbitrary Motion, Bremsstrahlung (Breaking Radiation), Cyclotron And Synchrotron Radiation, Radiation From Charges Moving In Matter

Unit - V
Relativistic Electrodynamics, The Special Theory Of Relativity, Covariant Classical Mechanics, Covariant Classical Electrodynamics,

Unit – VI
Electromagnetic Fields and Particles, Charged Particles In An Electromagnetic Field, Covariant Field Theory

References
4. "Feynman Lectures of Physics (Vol 2)", Feynman, Addison Wesley Publications, 2005
OBJECTIVES
To study different types of mixed signal VLSI design and their procedures with methods applied in different stages of design.

Unit - I

Unit - II
Data Converter SNR: Effective number of bits Clock jitter, Using averaging to improve SNR, Decimating filters for ADCs, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

Unit - III

Unit - IV
Implementing Data converters: Current mode and voltage mode R-2R DAC, Using Op-Amps in data converters, Implementing ADCs, Cyclic ADC, Introduction to Sigma Delta ADC and Line Drivers.

Unit - V
Integrator Based CMOS Filters: Integrator Building Blocks, Low pass and Active R-C filters, MOSFET-C integrators.

Unit - VI
Bilinear and Bi-quadratic transfer functions – Active R-C Transconductor-C and Switched Capacitor implementations both transfer functions, Canonic form of a digital filter.

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**OBJECTIVES**

The course provides the basics of network resilience and outlines its advantages and drawbacks. The interaction with other layers resilience schemes is also evaluated.

**Unit - I**

Terminology, Introduction to the different concepts related to resilience. Resilience, survivability, reliability, availability, protection, restoration.

**Unit - II**

Resilient technique basics. Protection and restoration schemes: dedicated, shared, path, span, link, segment, p-cycles. Resilient techniques in SONET/SDH and in the Optical Layer.

**Unit - III**

Resilient network static design. Techniques for designing resilient networks: Integer Linear Programming, Heuristics

**Unit - IV**


**Unit - V**

Resilient network time domain analysis: recovery time. Difference between static and dynamic resilient schemes: dynamic protection and restoration. Failure detection, failure notification, failure recovery. Relationship between statistical and time domain analysis.

**Unit - VI**

Multi-layer resilience. IP and MPLS resilience. Interaction with other layer’s resilient schemes (e.g., application layer resilience). Fault management. Control plane support for resilience. Quality of Resilience: Quality of Service in Resilience.

**References :**

OBJECTIVES
The primary objective of this course is to develop the ideas of optimality and adaptation in signal processing, design, analysis, and implementation of digital signal processing systems.

Unit – I

Unit – II

Unit – III

Unit – IV

Unit – V

Unit – VI

References:
OBJECTIVES
To introduce students to the embedded systems, its hardware and software, real time operating systems, inter-
task communication and an exemplary case of RTOS.

Unit I:
Introduction to embedded systems, basic concepts, definition, application areas and categories of embedded
systems: Stand alone Embedded systems, Real Time systems, Requirements, challenges Recent trends and
applications of Embedded systems.

[6 Hrs]

Unit II:/New trends in hardware platforms for Embedded system design, Processor selection criteria in Embedded
system design, Embedded system design with microcontrollers, 16 and 32 bits processor, DSP processor
and fuzzy controllers.

[7 Hrs]

Unit III:
Issues involved in choosing appropriate development platforms and tools for design of Embedded systems,
development environments, operating systems, task scheduling, non real and real time operating systems

[6 Hrs]

Unit IV:
Need for communication Interfaces, RS 232 communication parameters, connector configurations, UART,
serial communications, Ethernet, IEEE 802.11, Bluetooth system specifications

[6 Hrs]

Unit V:
Embedded Real Time Operating systems, concepts, architecture of Kernel, tasks, task scheduler, interrupt
service routines, semaphores, Mutex, Mailboxes, Message queue management function calls, event register
management function calls, signals and timer management function calls, memory management, priority
inversion problems in design of Embedded Real Time Operating systems.

[6 Hrs]

Unit VI:
Commonalities of Embedded Real Time Operating systems, Embedded operating systems – Embedded NT,
LINUX, Real Time Operating systems – QNX, RT LINUX, Concept of system on chip and system on Slice.

[6 Hrs]

Reference:
1. ‘Embedded / Real Time Systems – Concepts, design and programming’ Dr.K.V.K.K.Prasad, (DreamTech
3. ‘Programming for Embedded systems – Cracking the code’ DreamTech Software Team, WileyPublishing
Inc, 2006
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**OBJECTIVES**
EE 941 Project Phase – II

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OBJECTIVES